

Appl. No. 09/737,606

IN THE CLAIMS

1. (Currently Amended) A wafer for fabricating integrated circuits using a stepper, said wafer comprising:

a first region of the wafer, the first region having four sides and having for receiving a four-sided stepper shot, said stepper shot having a scribe line along each of the four sides of the first region its perimeter; and

four alignment targets disposed within said scribe line, said alignment targets for aligning said stepper shot and said first region;

wherein one alignment target is located on each of the four sides of the first region of said of said stepper shot, and wherein an first alignment target on a first side of said stepper shot the first region and an second alignment target on a second side of said stepper shot the first region opposing said first side are located in mirror-image positions, and wherein the second alignment target has a width that corresponds to a stepper rotational error between the first region and an adjacent second region of the wafer.

2. (Currently Amended) The wafer as recited in Claim 1 wherein opposing sides of the first region said stepper shot are equal in length, and wherein an alignment target is located at each mid-point of a side of said stepper shot.

3. (Currently Amended) The wafer as recited in Claim 1 wherein an alignment target is located at each corner of the first region said stepper shot.

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4. (Original) The wafer as recited in Claim 1 wherein said alignment targets are formed according to a positive resist process.

5. (Original) The wafer as recited in Claim 1 wherein said alignment targets are formed according to a negative resist process.

6. (Cancelled)

7. (Original) The wafer as recited in Claim 1 wherein each of said alignment targets comprise a plurality of rectangles.

8. - 20. (Cancelled)

21. (New) A semiconductor structure, comprising:

a wafer;

a plurality of four-sided integrated circuit regions, separated by scribe lines disposed on a first surface of the wafer; and

at least one alignment target disposed in a first scribe line, the first scribe line being a common region between a first stepper shot and a second stepper shot;

wherein the at least one alignment target has a width that corresponds to a stepper rotational error between the first stepper shot and the second stepper shot.